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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/733,953
Filing Date: December 10, 2003
Appellant(s): ARIMILLI ET AL.

Brian F. Russell
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/30/2010 appealing from the Office action mailed 03/04/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims pending on the application: 1-6 and 8-24.

Claims rejected: 1-6 and 8-24.

Claims on appeal: 1-6 and 8-24.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

6,697,919	Gharachorloo et al.	2-2004
2002/0178349	Shibayama et al.	11-2002
2003/0154351	Nilsson et al.	8-2003
2003/0033510	Dice	2-2003
5,926,831	Revilla et al.	7-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6 and 8-11, 13-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gharachorloo et al. (US Patent No. 6,697,919) in view of Shibayama et al. (US Publication No. 2002/0178349).

(1) regarding claim 1:

With respect to claim 1, Gharachorloo et al. teaches a data processing system (See FIG. 1), comprising: a system memory (see Fig. 1, memory subsystem 123); a plurality of processing cores (see column 4, lines 57-58, "...has eight processor cores"); a plurality of cache memories (see Fig. 1, caches 108, 110 and 114), wherein the plurality of cache memories temporarily hold cache lines of data identified by addresses of storage locations in the system memory and certain service memory access request receive via the interconnect that target those addresses (see column 9, lines 11-15; and column 18, lines 16-34); and a memory controller, (see column 4, line 49, "...memory controller". See FIG. 1) coupled to said interconnect and to the system memory (see column 4, lines 63-column 51 line 23. See also FIG. 1, element 118 connected to memory 123 and element 112 through element 114), that controls access to the system memory (see

column 5, lines 4-7, "Memory controller (MC) 118 that preferably interfaces directly to a memory bank of DRAM (dynamic random access memory) chips...in a memory subsystem 123"), wherein said memory controller responsive to receipt of a memory access request broadcast the memory controller and the plurality of cache memories (see FIG. 1, element 102; and column 18, lines 16-34).

Gharachorloo et al. does not teach said memory controller having a memory speculation mechanism that stores historical information regarding whether prior memory accesses were serviced by accessing the system memory; said memory access request specifying a target memory address, if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing reference to said system memory; and if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

However, Shibayama et al. teaches said memory controller having a memory speculation mechanism that stores historical information regarding whether prior memory accesses were serviced by accessing the system memory (see page 5, paragraph 62, lines 14-25; speculative execution result history storage stores history information regarding whether prior memory accesses were serviced by accessing the system memory (i.e., prior success/failure results)); said memory access request specifying a target memory address (see page 5, paragraph 64) if

speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing reference to said system memory (see page 1, paragraph 11, lines 1-3; and page 5, paragraph 62, lines 14-31; if execution success/failure prediction indicates speculative access (i.e. success) the memory operation instructions (i.e., load/write instructions) are executed in a speculative execution); and if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory (see page 1, paragraph 11, lines 1-3; page 5, paragraph 62, lines 14-25 and 31-36; if execution success/failure prediction does not indicate speculative access (i.e. failure) the memory operation instructions (i.e., load/write instructions) are executed in a non-speculative execution).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the method taught by Gharachorloo et al. to include the above mentioned to improve the performance of microprocessors of data processing devices (see page 1, paragraph 1).

(2) regarding claim 9:

With respect to claim 9, Gharachorloo et al. teaches a memory controller (see column 4, line 49; memory controller) for controlling access to a system memory (see FIG. 1, element 123;

memory subsystem) of a data processing system (see FIG. 1), control logic, that responsive to receipt of a memory access request broadcast the memory controller and the plurality of cache memories (see FIG. 1, element 102; and column 18, lines 16-34).

Gharachorloo et al. does not teach a memory speculation mechanism that indicates whether or not to perform speculative access to the memory based upon historical information regarding whether prior memory accesses were serviced by accessing said system memory; said memory access request specifying a target system memory address; if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing reference to said system memory; and if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

However, Shibayama et al. teaches a memory speculation mechanism that indicates whether or not to perform speculative access to the memory based upon historical information regarding whether prior memory accesses were serviced by accessing said system memory(see page 5, paragraph 62, lines 14-25; speculative execution result history storage stores history information regarding whether prior memory accesses were serviced by accessing the system memory (i.e., prior success/failure results)); said memory access request specifying a target system memory address (see page 5, paragraph 64); if speculative access is indicated by the

memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing reference to said system memory (see page 1, paragraph 11, lines 1-3; and page 5, paragraph 62, lines 14-31; if execution success/failure prediction indicates speculative access (i.e. success) the memory operation instructions (i.e., load/write instructions) are executed in a speculative execution); and if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory(see page 1, paragraph 11, lines 1-3; page 5, paragraph 62, lines 14-25 and 31-36; if execution success/failure prediction does not indicate speculative access (i.e. failure) the memory operation instructions (i.e., load/write instructions) are executed in a non-speculative execution).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the method taught by Gharachorloo et al. to include the above mentioned to improve the performance of microprocessors of data processing devices (see page 1, paragraph 1).

(3) regarding claim 14:

With respect to claim 14, Gharachorloo et al. teaches a memory controller (see column 4, line 49; memory controller) for controlling access to a system memory (see FIG. 1, element 123; memory subsystem) of a data processing system (see FIG. 1), control logic, that responsive to

receipt of a memory access request broadcast the memory controller and the plurality of cache memories (see FIG. 1, element 102; and column 18, lines 16-34).

Gharachorloo et al. does not teach said memory controller storing in a memory speculation mechanism historical information regarding whether or not prior memory accesses were serviced by access to the system memory (see page 5, paragraph 62, lines 14-25; speculative execution result history storage stores history information regarding whether prior memory accesses were serviced by accessing the system memory (i.e., prior success/failure results)); in response to a memory access request specifying a target system memory address (see page 5, paragraph 64); if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing reference to said system memory(see page 1, paragraph 11, lines 1-3; and page 5, paragraph 62, lines 14-31; if execution success/failure prediction indicates speculative access (i.e. success) the memory operation instructions (i.e., load/write instructions) are executed in a speculative execution); and if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory(see page 1, paragraph 11, lines 1-3; page 5, paragraph 62, lines 14-25 and 31-36; if execution success/failure prediction does not indicate speculative access (i.e. failure) the memory operation instructions (i.e., load/write instructions) are executed in a non-speculative execution).

However, Shibayama et al. teaches said memory controller storing in a memory speculation mechanism historical information regarding whether or not prior memory accesses were serviced by access to the system memory; in response to a memory access request specifying a target system memory address; if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing reference to said system memory; and if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the method taught by Gharachorloo et al. to include the above mentioned to improve the performance of microprocessors of data processing devices (see page 1, paragraph 1).

(4) regarding claim 2:

With respect to claim 2, Gharachorloo et al. teaches wherein said memory controller and said one or more processing cores are integrated within a same integrated circuit chip (see column 2, lines 10-14, "...the Alpha 21364 aggressively exploits semiconductor technology trends by including a scaled 1 GHz 21264 core, two levels of caches, memory controller, coherence hardware, and network router all on a single die..." See FIG. 1).

(5) regarding claims 3, 10 and 15:

With respect to claims 3, 10 and 15, Gharachorloo et al. teaches wherein said memory speculation mechanism comprises a memory speculation table ("directory", See rejection of claim 1 and FIGs. 4 and 10c) that stores a respective memory access history ("Directory Entry" of FIG. 4) for each of a plurality of threads executing within said one or more processing cores["simultaneous multithreading (SMT)" is disclosed in column 2, line 29. Also in column 1, lines 33-34, "instruction-level parallelism and speculative out-of-order execution" which teach this limitation).

(5) regarding claims 4, 11 and 16:

With respect to claims 4, 11 and 16, Gharachorloo et al. teaches wherein said system memory (see FIG. 1, element 123) includes a plurality of storage locations (see abstract; "memory line") arranged in a plurality of banks (see column 5, lines 1-8; "each memory bank"), and wherein said memory speculation mechanism (see abstract; "directory") stores said historical information on a per-bank basis (see column 11, lines 56-61: "...the memory line address identifies the node 102, 104 that interfaces with the memory subsystem 123 that stores the memory line of information 184 (i.e., home node) and a specific position within the memory subsystem 123 of the memory line information." Also see column 5, lines 3-7; MC 118 interfaces directly with a memory bank in memory subsystem 123).

(6) regarding claim 6:

With respect to claim 6, Gharachorloo et al. teaches wherein said system memory comprises a first system memory (see column 4, lines 63-67 - column 5, lines 1-8, "memory bank"); said memory controller comprises a first memory controller (see column 4, lines 63-67 - column 5, lines 1-8, "memory controller"); said data processing system further comprising a second system memory and a second memory controller that controls access to the second system memory (see column 4, lines 63-67 - column 5, lines 1-8, that each (1st, 2nd, etc...) processor core has its own memory (L1 cache, L2 cache, memory bank of DRAM) as well as memory controller. See FIGs. 1 and 2); said memory controller speculatively initiates access to said first system memory based upon historical information recorded by said second memory controller (see column 21, lines 59-63, "The present invention includes a cache coherence protocol (CCP) that enables the sharing of memory lines of information 184 across multiple nodes 102, 104." Gharachorloo teaches that memory speculation can be accessed by another node (processor core, memory controller, etc.: element 102 of FIG. 1) through CCP. Also see limitation in rejection of claim 1 (also interpreted under 35 U.S.C. 112 6th paragraph) With respect to the limitation, "based upon historical information recorded by said second memory controller", the examiner notes that a second memory controller can be any of a plurality of memory controllers and therefore is interpreted as analogous to claim 1).

(7) regarding claim 8:

With respect to claim 8, Gharachorloo et al. teaches response logic that provides said coherency message for said memory access request (see column 23, lines 14-60).

(5) regarding claim 13:

With respect to claim 13, Gharachorloo et al. teaches wherein said control logic speculatively initiates access to said system memory based upon historical information recorded by another memory controller of another system memory (see column 21, lines 59-63, "The present invention includes a cache coherence protocol (CCP) that enables the sharing of memory lines of information 184 across multiple nodes 102, 104." Gharachorloo teaches that memory speculation can be accessed by another node (processor core, memory controller, etc.: element 102 of FIG. 1) through CCP).

(5) regarding claim 18:

With respect to claim 18, Gharachorloo et al. teaches wherein said control logic speculatively initiates access to said system memory based upon historical information recorded by another memory controller of another system memory (see column 21, lines 59-63, "The present invention includes a cache coherence protocol (CCP) that enables the sharing of memory lines of information 184 across multiple nodes 102, 104." Gharachorloo teaches that memory speculation can be accessed by another node (processor core, memory controller, etc.: element 102 of FIG. 1) through CCP).

Claims 5, 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gharachorloo et al. (US Patent No. 6,697,919), Shibayama et al. (US Publication No. 2002/0178349) as applied to claims 1, 9 and 14 above, and further in view of Nilsson et al. (US 2003/0154351).

(1) regarding claims 5, 12 and 17:

With respect to claims 5, 12 and 17, Gharachorloo et al. and Shibayama et al. do not teach wherein said coherency message comprises a combined response representing a systemwide response to said memory access request.

However, Nilsson et al. teaches wherein said coherency message comprises a combined response representing a systemwide response to said memory access request (see page 3, paragraph 26).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the method taught by Gharachorloo et al. and Shibayama et al. to include the above because in that way subsequent memory access request latencies can be reduced (see page 1, paragraph 7, lines11-13).

Claims 19, 21 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gharachorloo et al. (US Patent No. 6,697,919), Shibayama et al. (US Publication No. 2002/0178349) as applied to claims 1, 9 and 14 above, and further in view of Dice (US 2003/0033510).

(1) regarding claims 19, 21 and 23:

With respect to claims 19, 21 and 23, Gharachorloo et al. and Shibayama et al. do not teach wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory.

However, Dice teaches wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory (see page 4, paragraph 39; pages 6 and 7, paragraph 58-60 and page 8, claim 11; system uses a MESI coherency protocol to update or change a coherency indicator that indicates if speculative execution is allowed or not (i.e., correct or not)).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the method taught by Gharachorloo et al. and Shibayama et al. to include the above prevent corrupting data or losing data.

Claims 20, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gharachorloo et al. (US Patent No. 6,697,919), Shibayama et al. (US Publication No. 2002/0178349) as applied to claims 1, 9 and 14 above, and further in view of Revilla et al. (US Patent No. 5,926, 831).

(1) regarding claims 20, 22 and 24:

With respect to claims 20, 22 and 24, Gharachorloo et al. and Shibayama et al. do not teach wherein the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request.

However, Revilla et al. teaches wherein the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request (see column 1,

lines 50-55 and column 5, lines 47-60; when a speculative access can deliver incorrect data a bit is sent to the memory controller to stop the speculative request and the data associated with the request is not used).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the method taught by Gharachorloo et al. and Shibayama et al. to include the above mentioned to avoid losing information or corrupting data (see column 2, lines 15-20).

(10) Response to Argument

Appellant, in I(A)(1)(a), argues that the combination of Gharachorloo and Shibayama do not teach memory controller having a memory speculation mechanism that stores historical information regarding whether prior memory accesses were serviced by accessing the system memory as recited in claim 1.

In response: The examiner disagrees with this statement. Shibayama et al. teaches a memory controller (i.e., processor) (see page 5, paragraph 62, lines 5-8) having a memory speculation mechanism (see page 5, paragraph 62, lines 1-8; processor having a function for executing memory operations instructions by means of speculative execution) that stores historical information (see page 5, paragraph 62, lines 5-7; processor comprises speculative execution result history) regarding whether prior memory accesses were serviced by accessing the system memory (see page 5, paragraph 62, lines 14-25; speculative execution result history storage stores history information regarding whether prior memory accesses were serviced by

accessing the system memory (i.e., if result is success the memory access was serviced by the system memory)).

Appellant, in I(A)(1)(b), argues that the Gharachorloo and Shibayama references are not properly combined because they would not have led to the claimed subject matter, and because of that claim 1 is not obvious in view of the combination of references because they do not teach a memory speculation mechanism that stores historical information regarding whether prior memory accesses were serviced by accessing the system memory.

In response: The examiner disagrees with this statement. The reason is discussed on the response to the arguments made in I(A)(1)(a).

Appellant, in I(A)(1)(c), argues that claim 1 is believed to be allowable for at least the same reasons as discussed in I(A)(1)(a) and I(A)(1)(b).

In response: The examiner disagrees with this statement. The reason is discussed on the response to the arguments made in I(A)(1)(a) and I(A)(1)(b).

Appellant, in I(A)(2), argues the combination of Gharachorloo and Shibayama do not teach if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing reference to said system memory; and if speculative access is not indicated by the memory speculation mechanism, initiates non-

speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory as recited in claim 1.

In response: The examiner disagrees with this statement. Shibayama et al. teaches if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message (see page 18, paragraph 237; and paragraph 238, lines 1-7; the processor is informed whether or not the memory access is going to be serviced (i.e., success/failure)) indicating whether or not said memory access request is to be serviced by the memory controller accessing reference to said system memory (see page 1, paragraph 11, lines 1-3; and page 5, paragraph 62, lines 14-31; if execution success/failure prediction indicates speculative access (i.e. success) the memory operation instructions (i.e., load/write instructions) are executed in a speculative execution); and if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory (see page 1, paragraph 11, lines 1-3; page 5, paragraph 62, lines 14-25 and 31-36; if execution success/failure prediction does not indicate speculative access (i.e. failure) the memory operation instructions (i.e., load/write instructions) are executed in a non-speculative execution).

Appellant, in I(B), argues the combination of Gharachorloo and Shibayama do not teach wherein said memory speculation mechanism comprises a memory speculation table that stores a

respective memory access history for each of a plurality of threads executing within said one or more processing cores as recited in claim 3.

In response: The examiner disagrees with this statement. Gharachorloo et al. teaches wherein said memory speculation mechanism comprises a memory speculation table ("directory", See rejection of claim 1 and FIGs. 4 and 10c; and column 10, lines 65-68 and column 11, lines 1-6; directory is in the protocol engine of processor 104, and handles the memory transactions) that stores a respective memory access history ("Directory Entry" of FIG. 4) for each of a plurality of threads executing within said one or more processing cores["simultaneous multithreading (SMT)" is disclosed in column 2, line 29. Also in column 1, lines 33-34, "instruction-level parallelism and speculative out-of-order execution" which teach this limitation).

Appellant, in I(C), argues the combination of Gharachorloo and Shibayama do not teach wherein said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis as recited in claim 4.

In response: The examiner disagrees with this statement. Gharachorloo et al. teaches wherein said system memory (see FIG. 1, element 123) includes a plurality of storage locations (see abstract; "memory line") arranged in a plurality of banks (see column 5, lines 1-8; "each memory bank"), and wherein said memory speculation mechanism (see abstract; "directory"; and column 10, lines 65-68 and column 11, lines 1-6; directory is in the protocol engine of processor 104, and handles the memory transactions) stores said historical information on a per-bank basis

(see column 11, lines 56-61: "...the memory line address identifies the node 102, 104 that interfaces with the memory subsystem 123 that stores the memory line of information 184 (i.e., home node) and a specific position within the memory subsystem 123 of the memory line information." Also see column 5, lines 3-7; MC 118 interfaces directly with a memory bank in memory subsystem 123).

Appellant, in I(D), argues the combination of Gharachorloo and Shibayama do not teach said memory controller speculatively initiates access to said first system memory based upon historical information recorded by said second memory controller as recited in claim 6.

In response: The examiner disagrees with this statement. Gharachorloo et al. teaches wherein said system memory comprises a first system memory (see column 4, lines 63-67 - column 5, lines 1-8, "memory bank"); said memory controller comprises a first memory controller (see column 4, lines 63-67 - column 5, lines 1-8, "memory controller"); said data processing system further comprising a second system memory and a second memory controller that controls access to the second system memory (see column 4, lines 63-67 - column 5, lines 1-8, that each (1st, 2nd, etc...) processor core has its own memory (L1 cache, L2 cache, memory bank of DRAM) as well as memory controller. See FIGs. 1 and 2); said memory controller speculatively initiates access to said first system memory based upon historical information recorded by said second memory controller (see column 21, lines 59-63, "The present invention includes a cache coherence protocol (CCP) that enables the sharing of memory lines of information 184 across multiple nodes 102, 104." Gharachorloo teaches that memory speculation can be accessed by another node (processor core, memory controller, etc.: element 102 of FIG.

1) through CCP. Also see limitation in rejection of claim 1 (also interpreted under 35 U.S.C. 112 6th paragraph) With respect to the limitation, "based upon historical information recorded by said second memory controller", the examiner notes that a second memory controller can be any of a plurality of memory controllers and therefore is interpreted as analogous to claim 1).

Appellant, in II, argues that Gharachorloo et al., Shibayama et al. and Dice do not teach wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as recited in claims 19, 21 and 23.

In response: The examiner disagrees with this statement. Dice teaches wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory (see page 4, paragraph 39; pages 6 and 7, paragraph 58-60 and page 8, claim 11; system uses a MESI coherency protocol to update or change a coherency indicator that indicates if speculative execution is allowed or not (i.e., correct or not)).

Appellant, in III, argues that Gharachorloo et al., Shibayama et al. and Revilla et al. do not teach wherein the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request as recited in claims 20, 22, 24.

In response: The examiner disagrees with this statement. Revilla et al. teaches wherein the memory controller, responsive to the coherency message indicating speculative access to the

system memory by the memory controller was incorrect, discards data associated with the memory access request (see column 1, lines 50-55 and column 5, lines 47-60; when a speculative access can deliver incorrect data a bit is sent to the memory controller to stop the speculative request and the data associated with the request is not used).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Aracelis Ruiz/

Examiner, Art Unit 2189

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2187

/Reginald G. Bragdon/
Supervisory Patent Examiner, Art Unit 2189